Exploiting eXascale Technology with Reconfigurable Architectures

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EXTRA partners
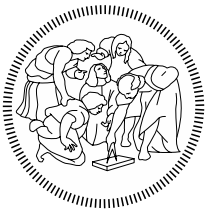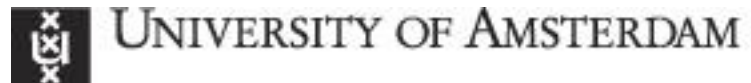
Reconfigurable Technology Basics

CPU

FPGA

Application
Software

F_2

Static

F_2

Reconfiguration
Request

config.
DB

Configuration
Manager

Configuration Interface
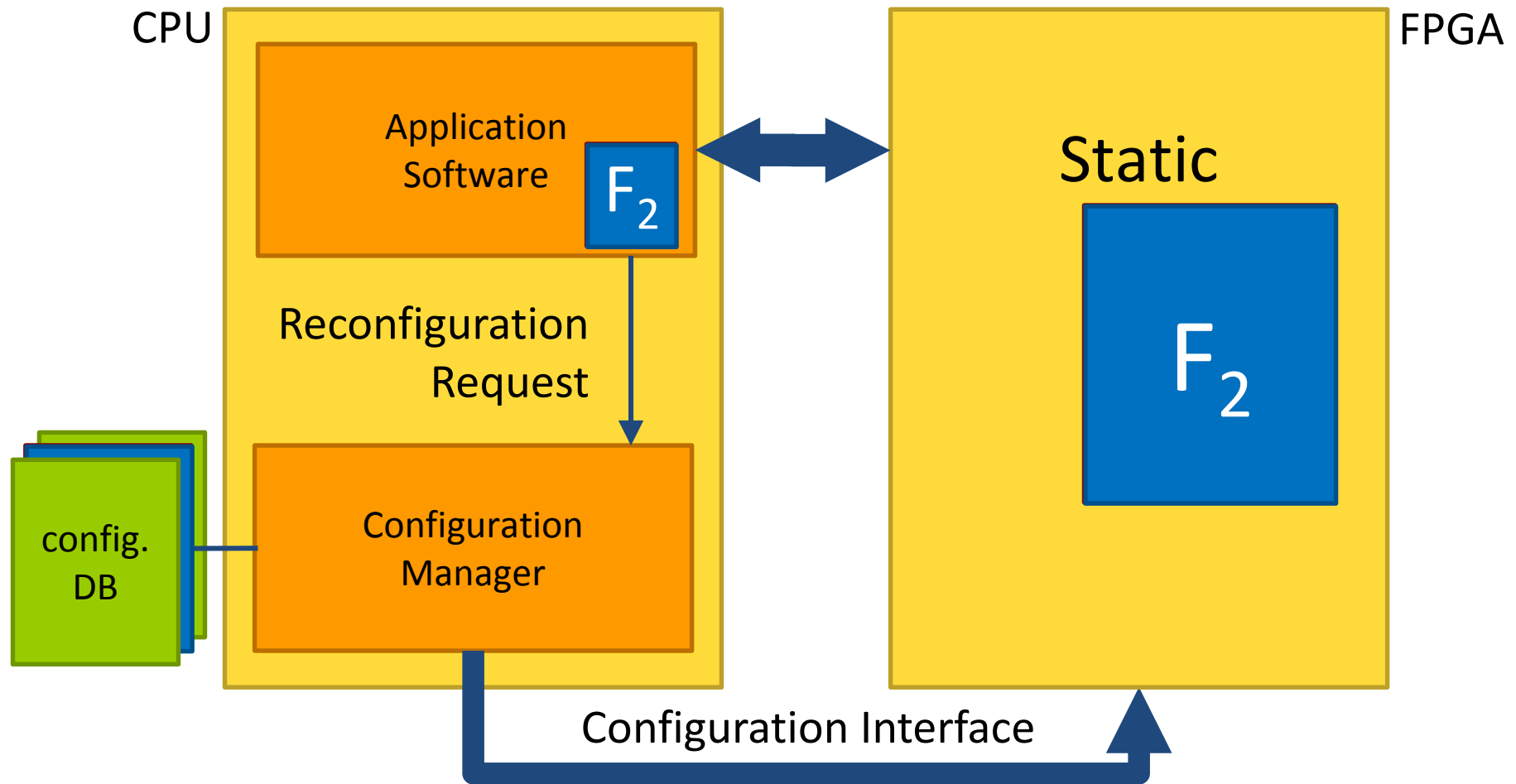
Reconfigurable Technology Basics

Technology for practical adaptable hardware systems

- Can add/remove components at run-time/product lifetime
  - Hardware can change post deployment
- Flexibility at hardware speed (not quite ASIC)
- Parallelism at hardware level (depending on application)
- Ideally: alter function & interconnection of blocks

Implementation in:

- FPGAs: fine grain, complex gate + memory + DSP blocks
- Coarse Grain (custom) chips: multiple ALUs, multiple (simple) programmable processing blocks, etc.

Exascale HPC Systems Challenges

- Power consumption of HPC systems skyrockets
  - Ever more compute intensive tasks

- Modern data centers
  - >50% power for non computing activities (including cooling)

- It is necessary to
  - Handle each task with near-optimal power efficiency
  - Adapt the system optimally to the needs of the application

- Heterogeneous Exascale HPC systems
  - Customize each node to the current task
  - Employ ultra-efficient compute nodes

Heterogeneous HPC Systems

- Envisioned nodes to improve the energy efficiency
  - High performance General Purpose Processors
  - Application specific hardware
    - Customized for specific computational kernels

- Run-time reconfigurability of hardware mandatory
  - Best for applications that significantly change during execution

- Implement applications on dedicated/reconfigurable HW
  - Higher energy efficiency
  - Less heat dissipation

- General Purpose Processors (GPPs) are still needed
  - Run the OS
  - Control the accelerators

Limitations of Existing Reconf. Syst.

- Reconfiguration overheads from the programming tools
- Run-time reconfigurable systems use existing FPGAs
  - Not specifically built with run-time reconfiguration in mind
  - Lack in efficiency for exploiting reconfiguration benefits
- The optimal reconfiguration granularity is undecided
  - Current FPGAs – higher flexibility, longer reconfiguration time
  - Coarser granularity – shorter reconfiguration time
- HPC applications do not fully exploit reconfigurability
  - The toolchains do not maximize
    - Programmability
    - Designer productivity
- EXTRA is here to address these problems

The EXTRA Project

- **E**xploiting e**X**ascale **T**echnology with **R**econfigurable **A**rchitectures

- Main objective:
  - Develop an open source research platform for continued research on reconfiguration architecture and tools

- Develop and program HW with run-time reconfiguration as a design concept

- Enable joint optimization of architecture, tools, applications and reconfigurable technology

- Prepare the HPC hardware nodes of the future

EXTRA project structure
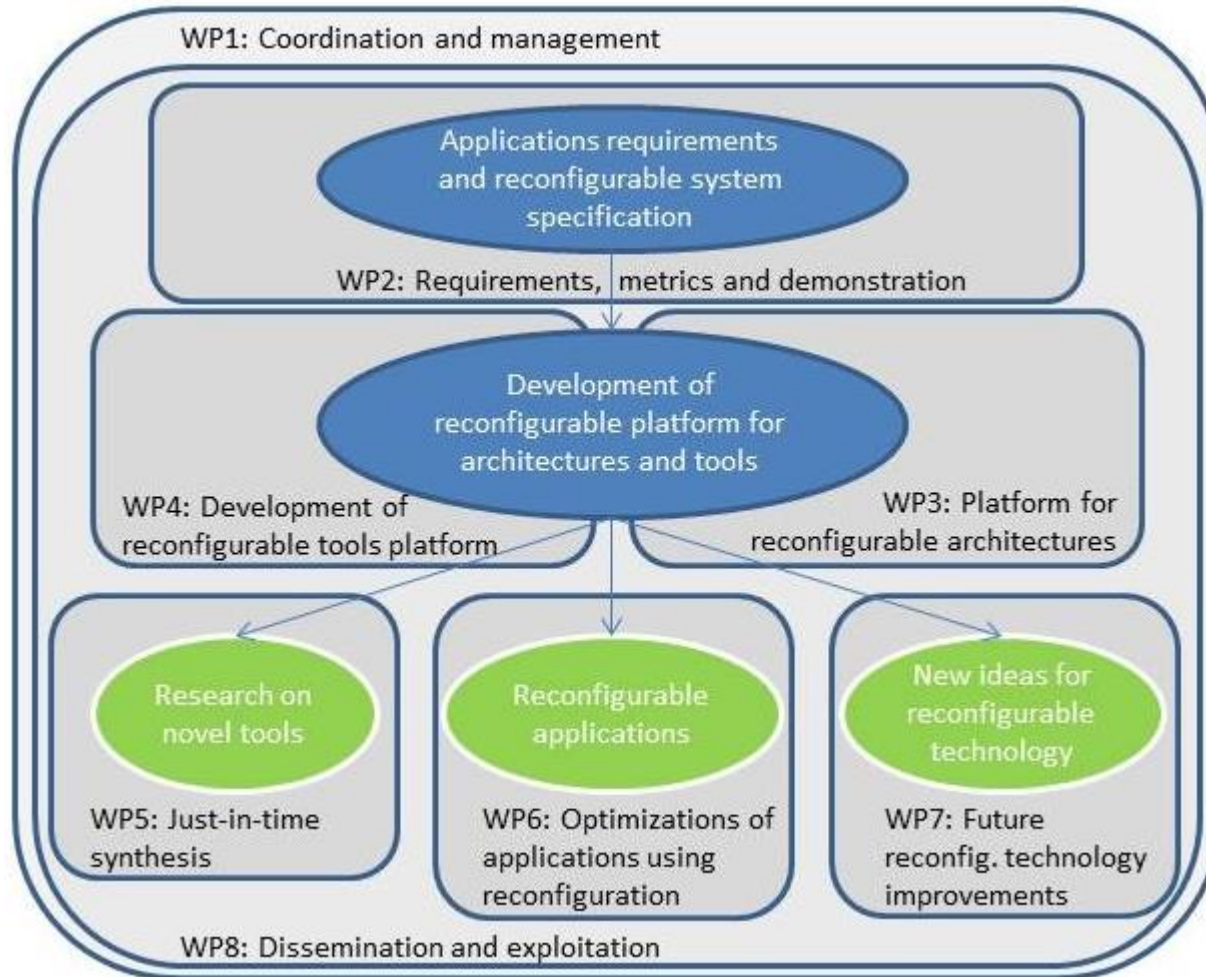
The basis of further work in the project

Open source platform for researchers

Improvements using the platform

Main Approach

- Reconfigurability - a key concept in future HPC systems
- To develop reconfigurable HPC systems we need to
    1. Design completely new inherently reconfigurable architectures
    2. Develop new tools that enable efficient reconfiguration
    3. Identify the applications that can best exploit reconfigurability

- EXTRA: minimize the reconfiguration overhead
    – Support run-time reconfiguration

Open research platform
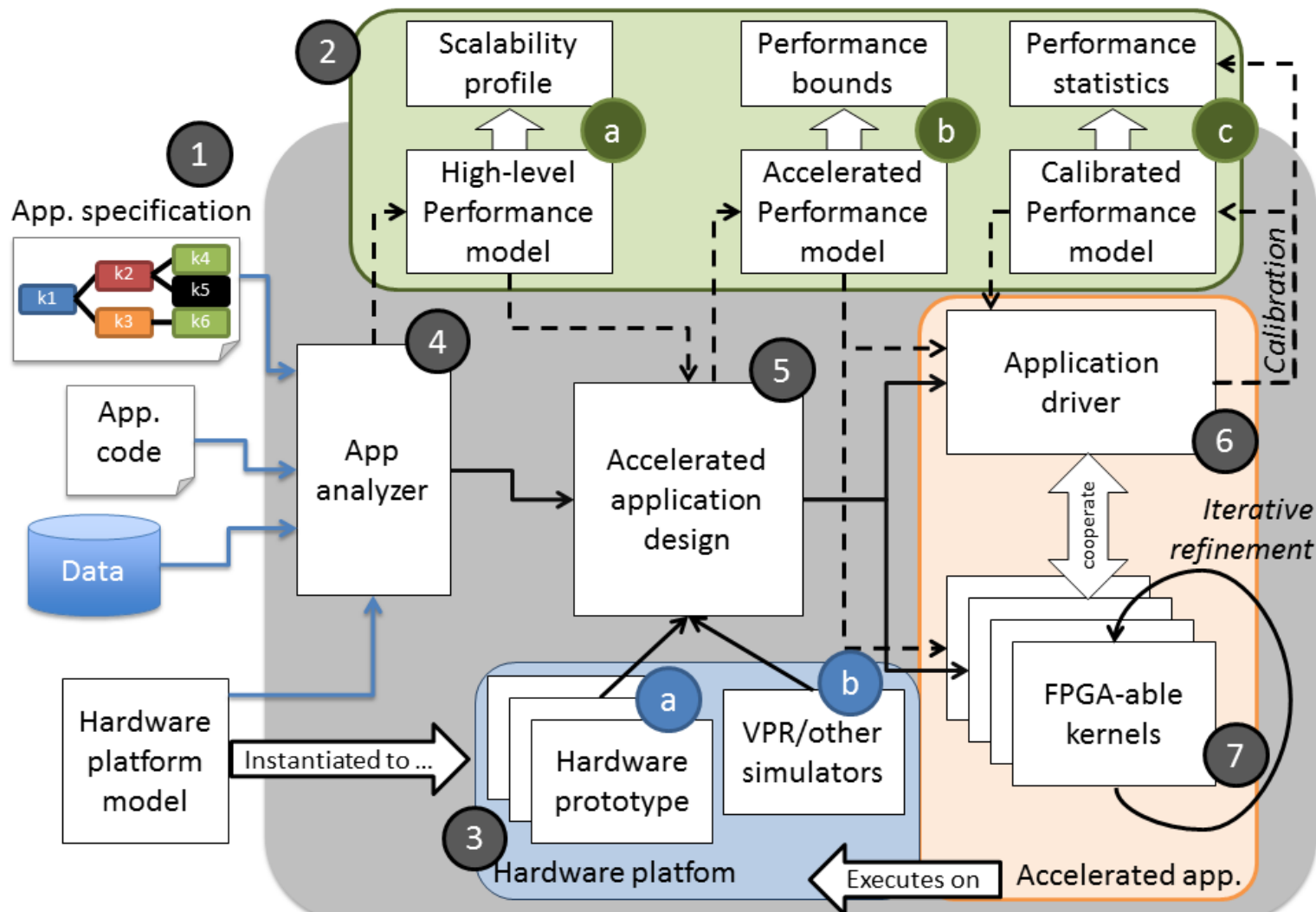
Demonstration and Use

- Demonstrate the effectiveness of the EXTRA platform for developing three complex applications from different application domains:
  - (a) Financial option pricing application (Maxeler)
  - (b) Retinal image segmentation (Synelixis)
  - (c) scientific applications: Quantum Monte Carlo (University of Cambridge)

- Evaluate the open research platform for reconfiguration and promote it to other researchers.
  - First contact with Research Advisory Board (RAB) and Industry Advisory Board (IAB) planned next month

EXTRA expected impact

- Strengthening European research and industrial leadership in HPC technologies

- Covering important segments of the broader and/or emerging HPC markets, especially extreme scale HPC systems

- Impact on standards bodies and other relevant international research programmes and frameworks

- European excellence in mathematics and algorithms for extreme parallelism and extreme data applications to boost research and innovation in scientific areas such as physics, chemistry, biology, life sciences, materials, climate, geosciences, etc.

Conclusions

EXTRA focuses on

- Building blocks for reconfigurable exascale HPC systems
- New architectures with low reconfiguration overhead
- New tools with reconfiguration as a design concept
- Applications exploiting run-time reconfiguration
- Exploration platform - smooth and efficient co-design of
  - Architecture
  - Tools
  - Applications

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