Welcome!

European Exascale Processor & Memory Node Design

http://exanode.eu/

ExaNoDe

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CEA

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Disclaimer: This presentation does not represent the opinion of the EC and the EC is not responsible for any use that might be made of information appearing herein.

- **Overview of the project:**
  - Objectives
  - Implementation

- **Technical backgrounds:**
  - Core technologies
  - Proof-of-Concept
  - Convergence with ETP4HPC SRA roadmap

- **Cooperation:**
 - With other European projects
 - ExaNoDe role for ESD

Vision, Core Technologies and Objectives

Vision for compute node

- Energy Efficiency.
- Dense Integration.
- Affordability.

Core Technologies for compute node

- ARMv8 based architecture.
- Integration technologies:
  - 3D integration/chiplet/interposer
  - Multi-chip-Module
- Virtualisation of system and resources:
  - Global Address Space (UNIMEM)
  - Virtualisation

Compute Unit example with 4 coherent islands
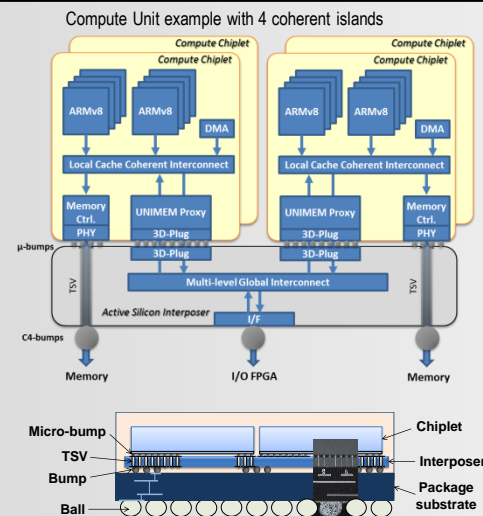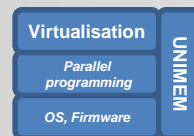
Project objectives

- **To validate** the ExaNoDe core technologies as enablers for European exascale HPC in an appropriately balanced integrated PoC solution.

- **To deliver a compute node** integrating core technologies consistent with the HPC system sizings and requirements for exascale computing.
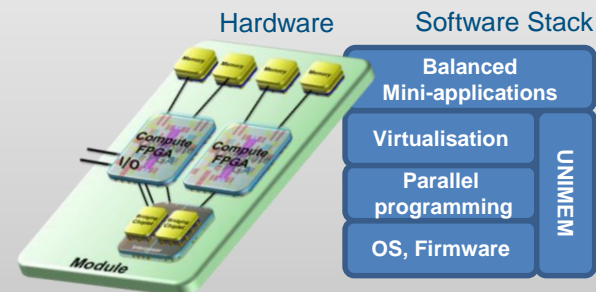
ExaNoDe Proof-of-Concept (PoC)

Project Implementation

T0: October 1st, 2015:
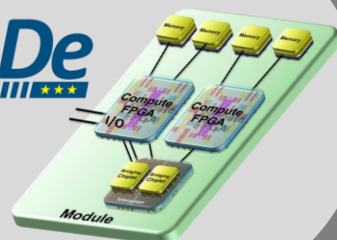**ExaNoDe @ Month 8**

Coordinator

CONSORTIUM

ExaNoDe

8.6 M€

IMPLEMEN-TATION

PROOF-OF-CONCEPT

WP1 : Management

WP2 : Co-Design for Exa-scale HPC systems

WP3 : Enablement of Software Compute Node

WP4 : Compute node design and manufacture

WP5 : System Integration & Evaluation

WP6 : Dissemination and Exploitation

Mini-applications-Design guidelines

SW eco-system

HW

Measure

Evaluation

Assessment

Balanced mini-apps

Virtualization

Parallel programming

OS, Firmware

UNIMEM
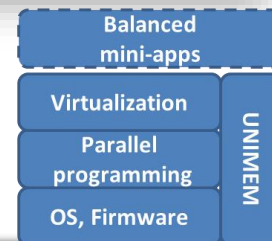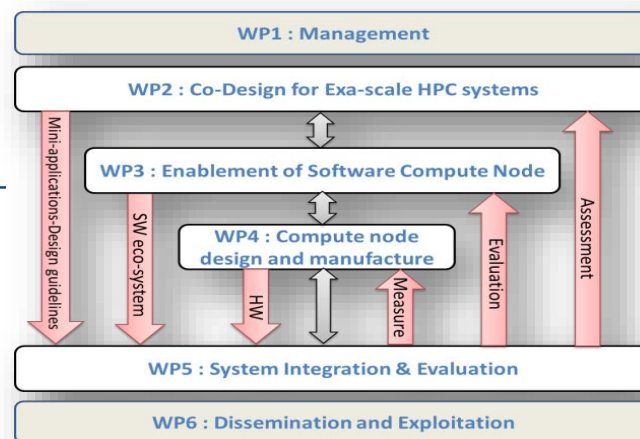
Compute Node

ExaNoDe prototype

ExaNoDe SW stack

ExaNoDe Core Technologies: Architecture

- **ARMv8 processors**
- **Scale-out architecture**
- **Global address space**

Compute Node example with 4 coherent islands
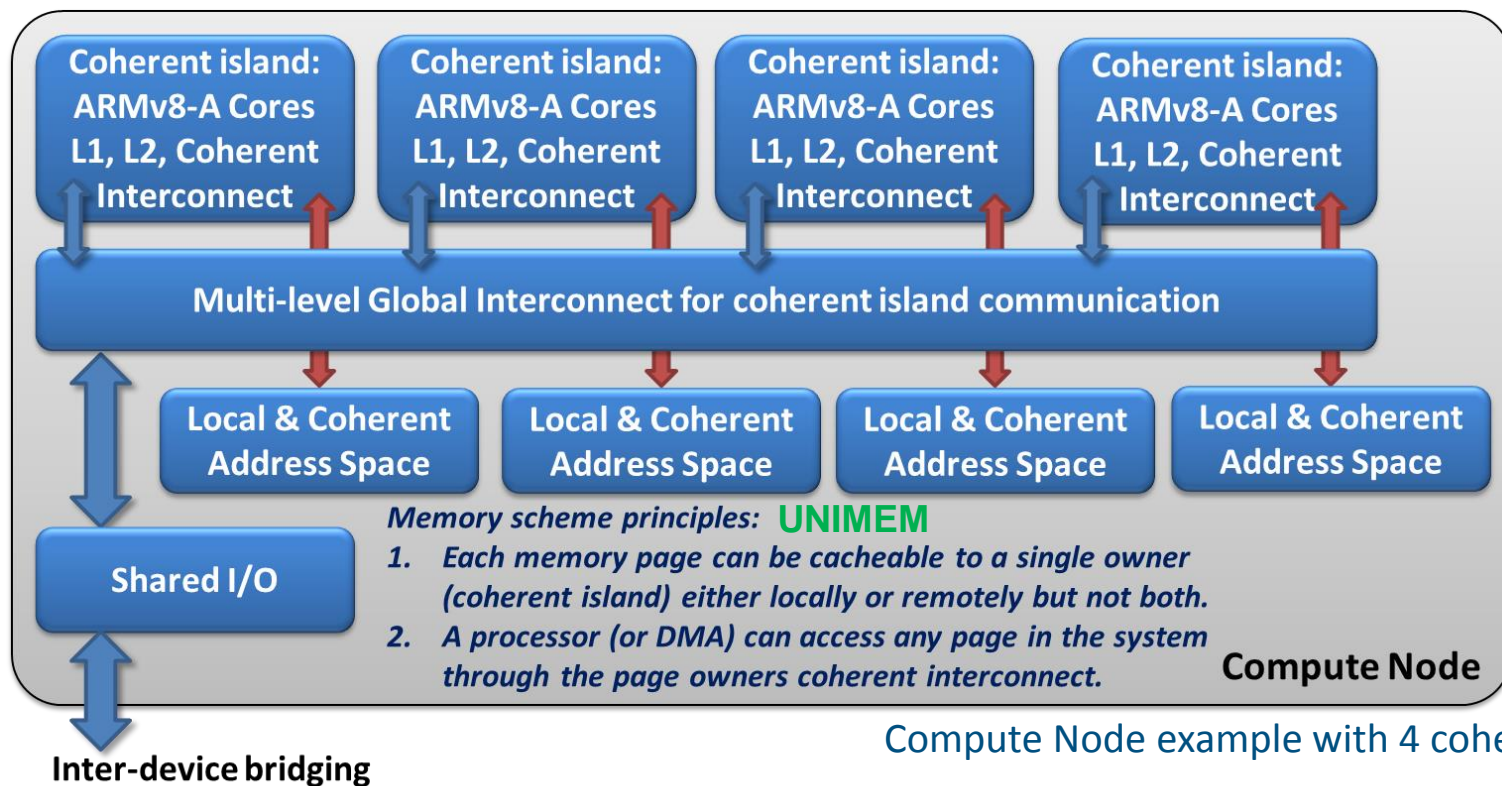
- **Chiplet on active interposer integration**
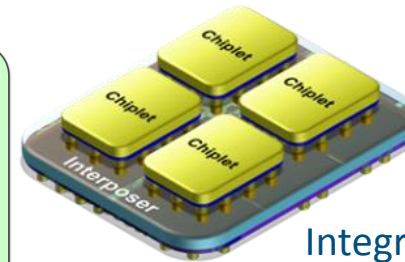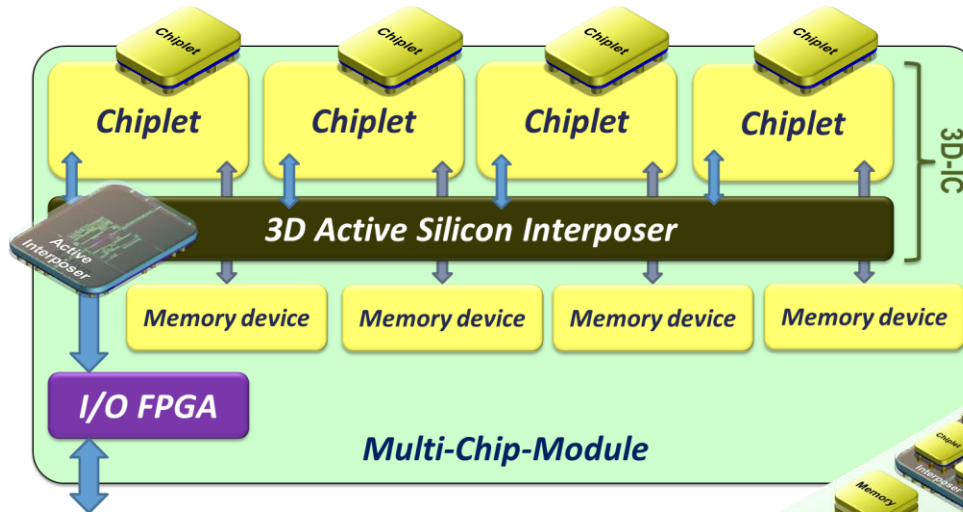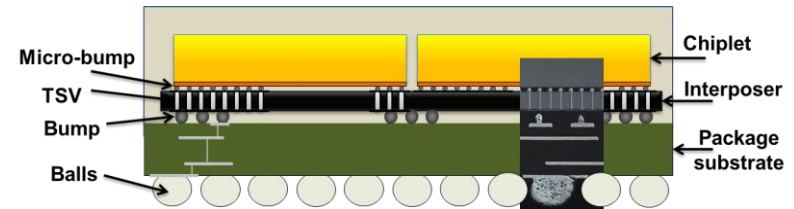
Integration partitioning example with 4 chiplets per 3D-IC and x2 3D-IC per module
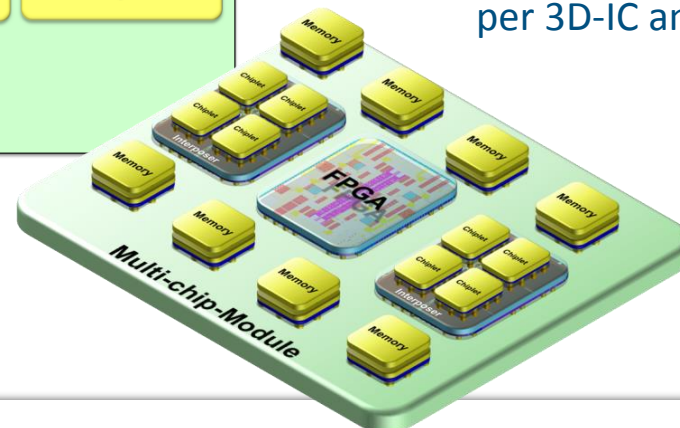
- **Multi-chip-Modules**

- **ExaNoDe application portfolio:**
  - Selection of the ExaNoDe mini-applications.
  - Co-design the ExaNoDe architecture.
  - Identify the critical kernels.

- **Deployment of a software ecosystem for the ARM-based Compute Node in conjunction with the UNIMEM system architecture.**

Balanced Mini-applications

Virtualisation

Parallel programming

OS, Firmware

UNIMEM

OmpSs
OpenStream
GPI-2
MPI
Linux KVM

Software Stack
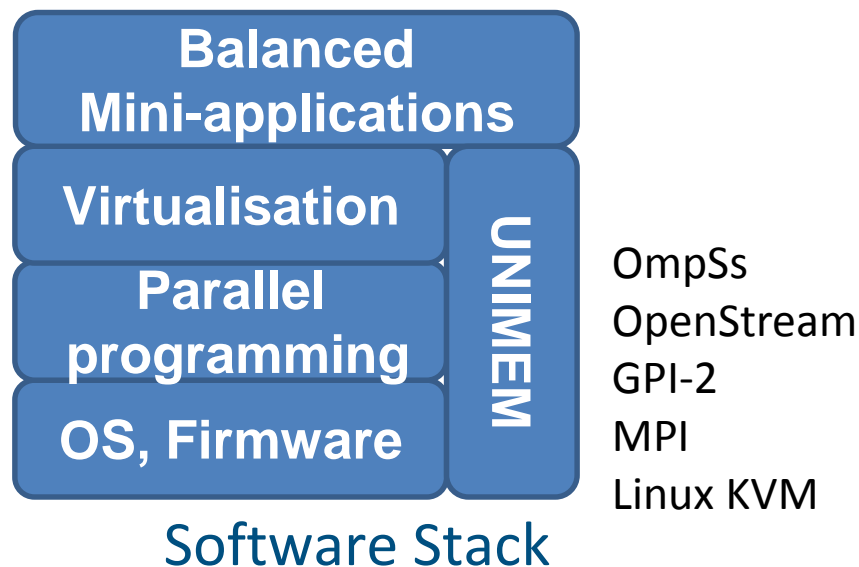
ExaNoDe realisation: Proof-of-Concept

- **Deliver a compute node integrating core technologies consistent with the HPC system sizings and requirements for exascale computing.**

- **Validate the ExaNoDe core technologies as enablers for European exascale HPC in an appropriately balanced integrated PoC solution.**

SW stack

Architecture: ARMv8, UNIMEM

Integration technology: Multi-chip-Module

Critical kernel from mimi-apps

Integration technology: active interposer and related design IPs in chiplet

Performance analysis
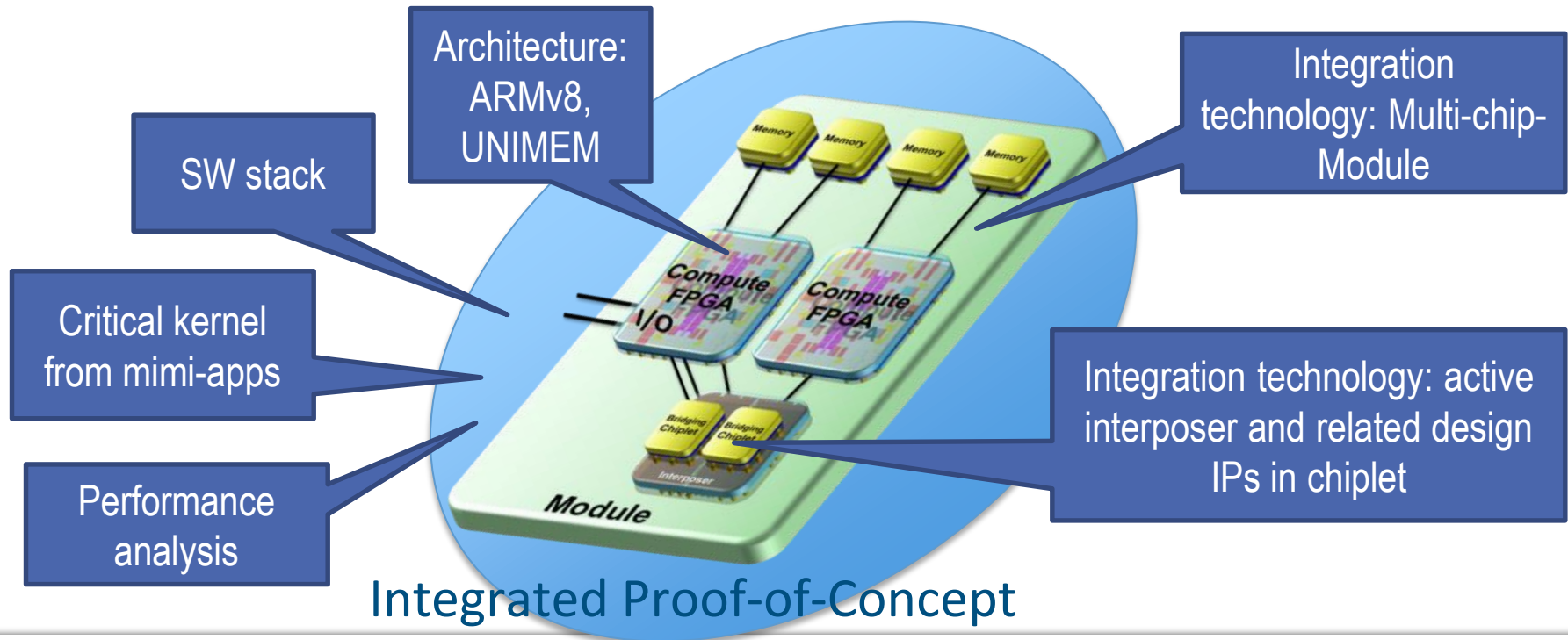
Integrated Proof-of-Concept

- Specification, Multi-board prototype.
- Preliminary SW.
- Mini-apps selection,
- Design guidelines.

Integrated Proof-of-Concept

How does it fit into ETP4HPC SRA roadmap ?

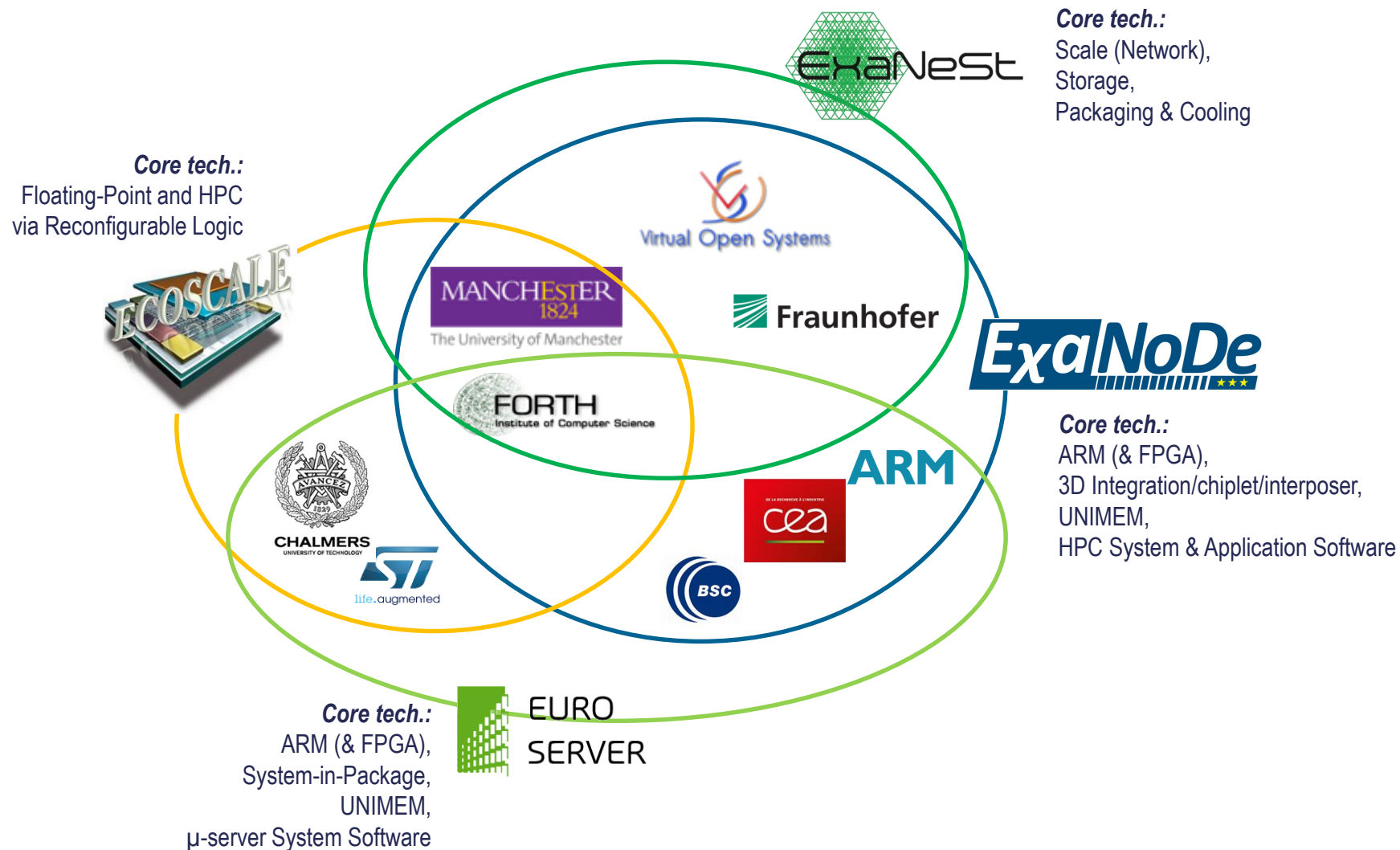| HPC SYSTEM ARCHITECTURE | SYSTEM SOFTWARE AND MANAGEMENT | PROGRAMMING ENVIRONMENT Including: Support for extreme parallelism | MATHEMATICS & ALGORITHMS FOR EXTREME SCALE HPC SYSTEMS — NEW — |

- ARMv8 based architecture
- UNIMEM memory scheme
- Heterogeneous architecture with interposer and Multi-Chip-Module
- Power efficient interfaces with active interposer
- Memory integration
- Energy efficiency
- Integration techno for new disruptive HPC architectures
- Intra-node interconnect management with active interposer and chiplet proxies
- Integration of balanced I/O

- System software and programming environment in the context of the capabilities of scalable many-core chips, heterogeneous compute elements, complex memory hierarchy, power efficiency constraints:
  - Firmware and OS
  - Virtualisation
  - Parallel programming models and runtime libraries
  - Evaluation of new memory management policies (Unimem)

ExaNoDe

ExaNoDe in European Cooperation Context

Core tech.:
Scale (Network),
Storage,
Packaging & Cooling

Core tech.:
Floating-Point and HPC
via Reconfigurable Logic

Core tech.:
ARM (& FPGA),
3D Integration/chiplet/interposer,
UNIMEM,
HPC System & Application Software

Core tech.:
ARM (& FPGA),
System-in-Package,
UNIMEM,
µ-server System Software

- **Core technology provider for HPC system architecture and components:**
  - System architecture:
    - Many-core architecture,
    - Heterogeneous architecture,
    - Memory management policies.
  - Components:
    - Integration technologies: active interposer, Multi-Chip-Module,
    - Design enablement solutions: libraries, IPs, methodologies.
  - Software enablement solutions:
    - Firmware and OS,
    - Virtualisation,
    - Parallel programming models and runtime libraries.

- **Evaluated in the context of HPC mini-applications with ExaNoDe PoC.**

- ➢ **To go toward an integrated compute node beyond the FPGA-version planned in the PoC.**

Thank you!

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