

Horizon2020 technology projects: how to increase their impacts

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Agenda

- FET HPC 2014
- FET HPC 2016
- FET HPC 2017
- ICT 11 2018
- Processor projects



HPC system oriented projects

- From silicon package to system
 - Interposer, UNIMEN architecture, interconnect, software stack
- ARM based HPC
 - Demonstrator and software stack
- Reconfigurable compute
 - Architecture, programming environment
 - Time constraint architecture
- IO
 - New memory hierarchy
 - File system













HPC stack and application oriented projects

- Energy efficiency
 - Metric, DSL, autotuning
- Programming models
 - OmpSs, StarPU, GASPI, PaRSEC, MPI, OpenMP
 - C++ templates + tool chain
- Deployment of multiscale applications
- Generic applications
 - Hyperbolic PDE
 - Fluid dynamics
 - Machine learning (for drug discovery)
 - Numerical linear algebra
 - Weather models























Quantitative analysis

- 171 IP (ie results) listed
- Most of them software related
 - 40 related to applications
 - Libraries
 - Runtime
 - FPGA tools and software
- Hardware results are divers
 - Boards: ARM, FPGA
 - Interconnect, cooling

HAPI	7
Happlication optimisation	7
⊞ benchmark suite	6
H demonstrator	8
H hardware	20
⊞ report	2
⊞software	114
± training	7
Total général	171



Who can (re-)use the results?

• Any member of the HPC ecosystem can take benefit from the outcomes of the projects

		application	benchmark	demonstr					Total
Étiquettes de lignes	▼ API	optimisation	suite	ator	hardware	report	software	training	général
application developer	7						39	4	50
application developer / computing centre				8			4	1	13
application developer / end user							10		10
computing centre		1	4				5		10
end user		6				2	34	2	44
ESD					4		5		9
HPC system customer					1				1
HPC system provider					13		9		22
HPC system provider/ application developer					1		3		4
HPC system provider/ computing centre			2				4		6
HPC system provider/ Processor provider					1		1		2
Total général	7	7	6	8	20	2	114	7	171



Demonstrators developed by the projects

- SAGE
 - Open to test; 4 tiers of storage
- NextGenIO
 - based on DC Persistent Memory[™] nextgeneration non-volatile memory technology



- Montblanc
 - Open to test; Dibona 96 sockets

ARM ThunderX2



- Exanode-ExaNest-EcoScale
 - Based on ExaNest daughter board
 - ~20 boards



- MANGO
 - 8 HPC servers and 196 FPGA



- Greenflash
 - To demonstrate control of telescope mirrors

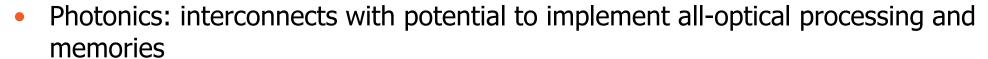


10 highlighted results











- HSM: tools to help manage data storage (for computing centres)
- API: Resource manager APIs: designed to permit multiple runtimes to negotiate access to hardware resources
- Power efficiency: Power management run-time for MPI-based applications
- Power efficiency: library for instrumentation, profiling and optimisation of HPC applications. Related tool performs the analysis of output data
- Math library: engine to solve hyperbolic systems of partial differential equations
- Math library: Communication avoiding iterative methods and their efficiency for solving linear elasticity problems









Key findings

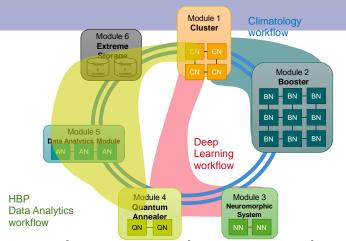
- Very rich reservoir
- Potential for integration projects:
 - Vertical a kind of Extreme Scale Demonstrators or now pilot systems
 - Horizontal to create European frameworks:
 - FPGA programming environment
 - Runtime
 - Energy management
- Continuation actions:
 - Dissemination
 - Continue the dialogue with the 2 co-design projects and the 11 FET HPC 2017 projects
 - Gap analysis compared to SRA 3



FET HPC 2016

DEEPEST

- Modular architecture
 - Booster concept
 - NAM: Network Attached Memory
 - IO: BeeGFS, SIONlib

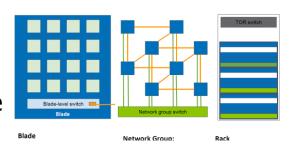




 Application co-design: high enrgy physic, climate simulation, CFD, brain simulation, seismic imageing, GROMACS, NEST (spiking NN), oil exploration, Lattice QCD, radio astronomy (SKA), Earthquake source dynamics, Earth science, electromagnetic, space weather, superconductivity

EuroExa

Based on UNIMEM architecture







- Cooling technology
- 14 applications: quantum expresso, NEMO, astronomy, NEST/DPSNN, FRTM, InfOli, SMURFE, AVU-GSR, IFS, LBM, Alya, GADGET, LFRic

FET-HPC-2017

1 Heterogeneous system management RECIPE

RECIPE

- 2 data IO oriented
 - SAGE2
 - **MAESTRO**
- 4 programming environment
 - Data: Aspide
 - Heterogeneous (CPU+GPU+FPGA): EPEEC, EPIGRAM-HS, EXA2PRO
- 2 Verification, Validation Uncertainty Quantification
 - ExaQUte
 - **VECMA**
- 1 visualization interactive HPC: VESTEC
- 1 Climate: ESCAPE2



















ICT 11 2018 Big Data and HPC

Cybele

- Precision Agriculture (PA) and Precision Livestock Farming (PLF) methods
- Use cases: organic soja, grape growth, fruit weather protection, crop yield forecasting, pig production, fishing, aquaculture

DeepHealth

- Deep learning and computer vision leading to European libraries
- 14 pilots
- Evolve
 - Testbed integrating HPC and BD techno
 - 10 proof of concepts
- LEXIS
 - Platform with data management and orchestration layers
 - Test bed: aeronautics, climate and weather, earthquake and tsunami





Leading the Big Data
Revolution





Processor

Montblanc 2020



- define a low-power System-on-Chip architecture targeting Exascale;
- implement new critical building blocks (IPs) and provide a blueprint for its first-generation implementation;
- deliver initial proof-of-concept demonstration of its critical components on real life applications;
- explore the reuse of the building blocks to serve other markets than HPC
- EPI
 - Target: HPC and automotive
 - Architecture: common platform with CPU and accelerator(s)





EPI common architecture

GPP AND COMMON ARCHITECTURE CCIX (RHEA) Kalray PCIe gen5 CCIX & CXL links links. (CRONOS) **ZEUS** (ARM) Dedicated D2D links cryptographic to adjacent chiplets 0 ASIC H eFPGA eFPGA **FPGA** HBM 2e memories Menta (FR) NOC - ARM - RHODES NoC GPP - ARM ZEUS ARM Rhodes DDR5 EPAC - EPI Accelerator (TITAN) memories MPPA - Multi-Purpose Processing Array eFPGA - embedded FPGA Cryptographic ASIC (EU Sovereignty) Any other ASIC Copyright © European Processor Initiative 2019. HSL: CCIX, CXL[Cronos] & PCIe5





Questions?

