



Extreme scale Demonstrators

- a project mgmt. view -

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the “Extreme scale Demonstrators” call

TOPIC : Co-designing Extreme Scale Demonstrators (EsD)

Topic identifier: ICT-14-2019

Publication date: 27 October 2017

Types of action: RIA Research and Innovation action

DeadlineModel: single-stage

Planned opening date: 26 July 2018

Deadline: 14 November 2018 17:00:00

Time Zone : (Brussels time)

..there might be delays in the opening and closing dates (shift to 2019).....

EXTREME-SCALE DEMONSTRATORS

HPC Centers

Participate in the co-design process
Manage system deployment
Operate
Validate and characterise the system

Technology Providers

Ensure the integration of the technologies
Perform the testing and quality/performance assurance
Perform the maintenance and service

1. Integrate results of R&D projects into fully integrated systems prototypes.
2. Establish proof-points for the readiness, usability and scalability of the technologies

Application owners

Define application requirements
Port and optimise applications

EsD 2018: (WP18)

- designpoint: 500-1000 PF
- power eff.: 35kW/PFLOPS
- density: 1PF/rack
- I/O balanced design
- TRL 7

7 EsD project challenges

(as discussed during EsD workshops and beyond)

1. Integrate results of R&D projects into fully integrated systems prototypes.

2. Establish proof-points for the readiness, usability and scalability of the technologies

3. EsD 2018: (WP18)
- designpoint: 500-1000 PF
 - power eff.: 35kW/PFLOPS
 - density: 1PF/rack
 - I/O balanced design
 - TRL 7

4. The project timing

Dev. / Integration / Test

Phase A: appr. 24 months

Install. / Benchmark & Use

Phase B: min. 24 months

5. Manage expectations of players:

- technology providers
- application owners
- HPC centers

6. Co-Design & Co-Dev.:

- System Architecture
- HW - development
- FW/OS adaption
- System integration
- Perf. modeling/benchm.
- Debug -tools dev. /adaption
- Application adaption/tuning
- Classical & System test
- Runtime & library-tuning
- Benchmark adaption
- Compiler adaption/tuning

7. The budget includes:

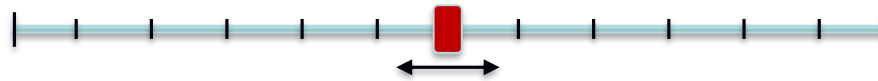
- entire R&D effort
- system procurement
- workload adaptations
- operational costs
- maintenance costs

...and there will be more !

Challenge 1

1. Integrate results of R&D projects into fully integrated systems prototypes.

Systems built out of commercially avail. subsystems and components
(R&I outside EU projects)



Systems built out of European Research results only

“Put the slider as far as possible to the right / as far as needed to the left”

Challenge 2

2. Establish proof-points for the readiness, usability and scalability of the technologies



➤ European Cloud Initiative:

- two exscale systems, one with European technology,
- two pre-exascale systems

EsDs to help establish tangible proof points at scale



Challenge 3

3. EsD 2018: (WP18)
 - designpoint: 500-1000 PF
 - power eff.: 35kW/PFLOPS
 - density: 1PF/rack
 - I/O balanced design
 - TRL 7

Discussed many times during EsD workshops:

- not a Linpack – machine only.....real applications matter!
- not highly tuned to only a few exotic applications
- ideal size around 5 % of top performance at the time of installation (2021)
- EsDs will have to be designed with a target performance of 500+ PFLOPs
- power efficiency: on path to exascale-goal: 50x - 100x of today's PRACE-Tier-0 performance within a power-envelope of 5...15 MW in 2024 (real appl.)
- packaging density: 1/3rd of exascale density in 2023/24
- BUT realistically: size might be determined by power budget of HPC centers!

Challenge 4

4. The project timing

Dev. / Integration / Test

Phase A: appr. 24 months

Install. / Benchmark & Use

Phase B: min. 24 months

- Phase A from start of project to completion of system test: appr. 24 months
- Phase B: code porting, dev., tuning, benchmarking, production: 24 months +

- Used technology must be mature enough and ready for integration at project start
- Analysis of system-design-point, technologies, integration & evaluation efforts already during proposal building
- Technology Readiness Level of 7 recommended to enable a stable and useful exploitation during phase B
- Technology providers (especially integrator) in support mode during entire phase B



Technology Readiness Levels

- TRL 0: Idea.** Unproven concept, no testing has been performed.
- TRL 1: Basic research.** Principles postulated and observed but no experimental proof available.
- TRL 2: Technology formulation.** Concept and application have been formulated.
- TRL 3: Applied research.** First laboratory tests completed; proof of concept.
- TRL 4: Small scale prototype** built in a laboratory environment ("ugly" prototype).
- TRL 5: Large scale prototype** tested in intended environment.
- TRL 6: Prototype system** tested in intended environment close to expected performance.
- TRL 7: Demonstration system** operating in operational environment at pre-commercial scale.
- TRL 8: First of a kind commercial system.** Manufacturing issues solved.
- TRL 9: Full commercial application,** technology available for consumers.

Challenge 5

5. Manage expectations of players:

- technology providers/integrators
 - application owners
 - HPC centers

Balancing priorities of the three main playing groups:

• **hosting HPC centers:**

- experimenting with new architectures,
- developing/benchmarking new applications, tools,
- keep maintenance and operational cost within acceptable limits

• **Applications owners:**

- developing new applications/tools based on new architectures
- porting / adapting existing applications/tools to new architectures,
- invest porting effort only in architectures that will lead to production systems
- system architecture and features of EsD must enable new problem solutions

• **Technology providers / Integrators**

- system design point compatible with own product line / option for commercialization
- resulting EsD system must be a meaningful step in own product line
- integration of mixed technology (own, external, FET/FP7-based) must be manageable

Challenge 6

6. Co-Design & Co-Development

- HPC centers, application owners, integrators and technology providers to co-design and co-develop during entire Phase A
- A very broad skills base required:
 - System Architecture
 - HW - development
 - FW/OS adaption
 - System integration
 - Perf. modeling/benchm.
 - Debug -tools dev. /adaption
 - Application adaption/tuning
 - Classical & System test
 - Runtime & library-tuning
 - Benchmark adaption
 - Compiler adaption/tuning
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- Special challenge for System Architect and Project Manager !

Challenge 7

7. The budget includes:

- entire R&D effort
- system procurement
- workload adaptations
- operational costs
- maintenance costs

- Cost management needs to cover mixed type of costs:
- Balance between:
 - operational costs in phase B ↔ R&D costs in phase A
(e.g. higher investment in energy efficiency R&D might reduce operational costs)
 - R&D and operational costs ↔ procurement costs
 - to be contained in budget as well:
 - Adaption/porting of workloads
 - Maintenance costs during phase B

Any questions?