



EuroLab-4-HPC

Foundations of a European Research Center of Excellence in HPC Systems

Coordinator: **Per Stenström**
Chalmers University of Technology
Sweden





Consolidation of HPC Systems Research in Europe

Before EuroLab-4-HPC:

- Key HPC stakeholder community (research, suppliers, users) was fragmented and uncoordinated
- **In particular:** Uncoordinated research community

EuroLab-4-HPC focus:

- Align research and other stakeholders around a common long-term research agenda
- Train future technology leaders
- Accelerate innovation in the HPC domain

***Vision: Making Europe a Leader in
HPC Technology***



EuroLab-4-HPC Achievements

Consolidation of research excellence in HPC systems

- **EuroLab HPC Vision:** a long-term research agenda
- A validated **HPC curriculum** and best practices
- Piloted **business prototyping** for accelerating innovations in HPC technologies
- **Ecosystem building:** Links to ETP4HPC, PRACE, EXDCI and other HPC stakeholders
- **Business model** for self-sustainability



Consortium

- Expertise spans system layers from applications via system software to platform architecture
- Strong links to HiPEAC, ETP4HPC, PRACE and EXDCI

CHALMERS



**Barcelona
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Centro Nacional de Supercomputación

H L R I S



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Agenda

- Research excellence
- Education
- Innovation
- Ecosystem building
- Concluding remarks





The EuroLab HPC Vision



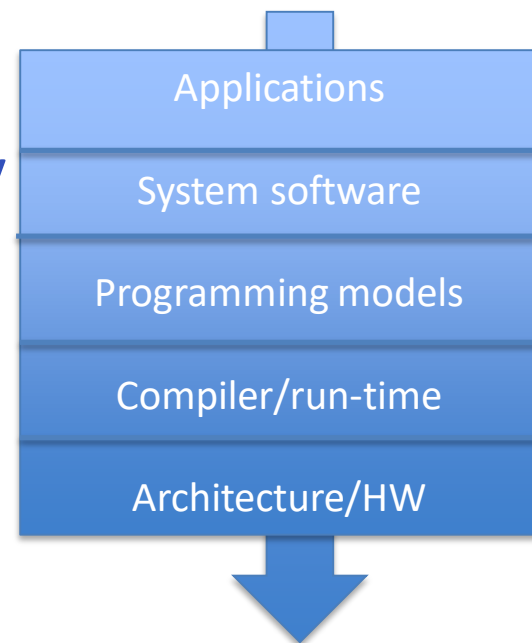


Roadmap Target

- Currently strong efforts are taken in US, China, Japan, and Europe towards the Exascale computers to be reached in 2020-2022.
- **Our objective:**
Long-term vision for excellence in European HPC research beyond Exascale targeting 2023—2030

EuroLab-4-HPC Roadmap Scope

- Include all layers of HPC stack
- **Cross-cutting issues:**
green ICT, energy and dependability
- **Adjacent domains:** high-performance embedded, data centres, big data
- Close collaboration with other roadmaps:
 - HiPEAC Vision,
 - ETP4HPC SRA – Strategic Research Agenda (until Exascale)





EuroLab-4-HPC Roadmap Approach

Long-term (2023-2030) => highly speculative:

1. Select disruptive technologies that may be technologically feasible in the next decade
2. Assess the potential hardware architectures and their characteristics
3. Assess what that could mean from different HPC perspectives (applications, software, architecture)
**"IF technology suitable
THEN foreseeable impact on HW/SW could be"**





Topics

- Disruptive Technologies
- New technologies and hardware architectures
- System software and programming environment
- Vertical challenges: Green ICT, energy and resiliency
- HPC applications: evolution and requirements
- Convergence of embedded HPC, data centers for big data, and HPC





Emerging Applications and SW Pull

For example,

- Data mining and analysis of big data
 - Pre- and post-processing, and data assimilation
- Real-time and interactive analysis and visualisation (Industry 4.0, smart cities, connected autonomous cars)
- Deep learning/neuromorphic
- Task parallelism replaces bulk synchronous
- New expert programming (DSLs)
- Approximate computing (concerns SW and HW)
- Homomorphic cryptography





Disruptive Technologies Push

- **Sustaining Technology** (improving HW in ways generally expected)
 - Continuous CMOS Scaling
 - Die Stacking - 3D-Chip
- **Disruptive Technology in Hardware/VLSI** (innovation that creates a new line of HPC HW superseding existing HPC techniques):
 - NVM Technologies (Memristors, STT-RAM)
 - Photonics
- **Disruptive technology** (alternative ways of computing)
 - Resistive Computing
 - Neuromorphic Computing
 - Quantum Computing
- **Beyond CMOS**
 - Nanotubes
 - Graphene
 - Diamond





Summary of Potential Long-Term Impacts of Disruptive Technologies for HPC Hardware

- **Processor Logic**
 - **Evolutionary:** CMOS technology may continuously scale in next decade to 8-4 nm
 - **Innovative:** Die stacking DRAM dies (Micron/Intel MCDRAM) and 3D many-core microprocessors with reduced wire length.
 - **Disruptive:** photons, graphene, or nanotube => much higher clock rates, less heat => disruptive change of computing.
- Memory Hierarchy
- Potential New Hardware Accelerators





HPC Curriculum and Best Practices

- Inventory of needs and supply of HPC courses for future HPC technology experts
- Focus is on
 - Defining an HPC curriculum
 - Best practices for on-line learning
 - Launch of training pilots

Outcome: Validated **HPC Curriculum** and **best practices** for on-line learning



HPC Curriculum

- **Analysis of requirements and input from:**
 - Partners from the project
 - Training providers PRACE, ACM SIGPLAN HPC, EIT ...
 - Online survey used to gather responses from individuals
- **Course inventory:** identification of existing courses and programmes
- **Proposals of core & supplemental courses**
 - Mapping courses to potential programs
 - Broader educational goals of the curriculum
 - Potential attendees considered EE/CS/Maths/Physics majors
 - Duration of program studies 2 years versus 1 year





HPC Curriculum

- Parallel Computer Architectures
- Scalable parallel algorithms
- Programming with MPI
- Data Parallel Computing
- Programming Shared Memory Parallel Systems
- Programming Multi-core and Many-core Systems
- Performance Engineering
- Programming Heterogeneous and Accelerated Systems
- Large scale Scientific Computation
- Data Science Fundamentals

Courses span across layers



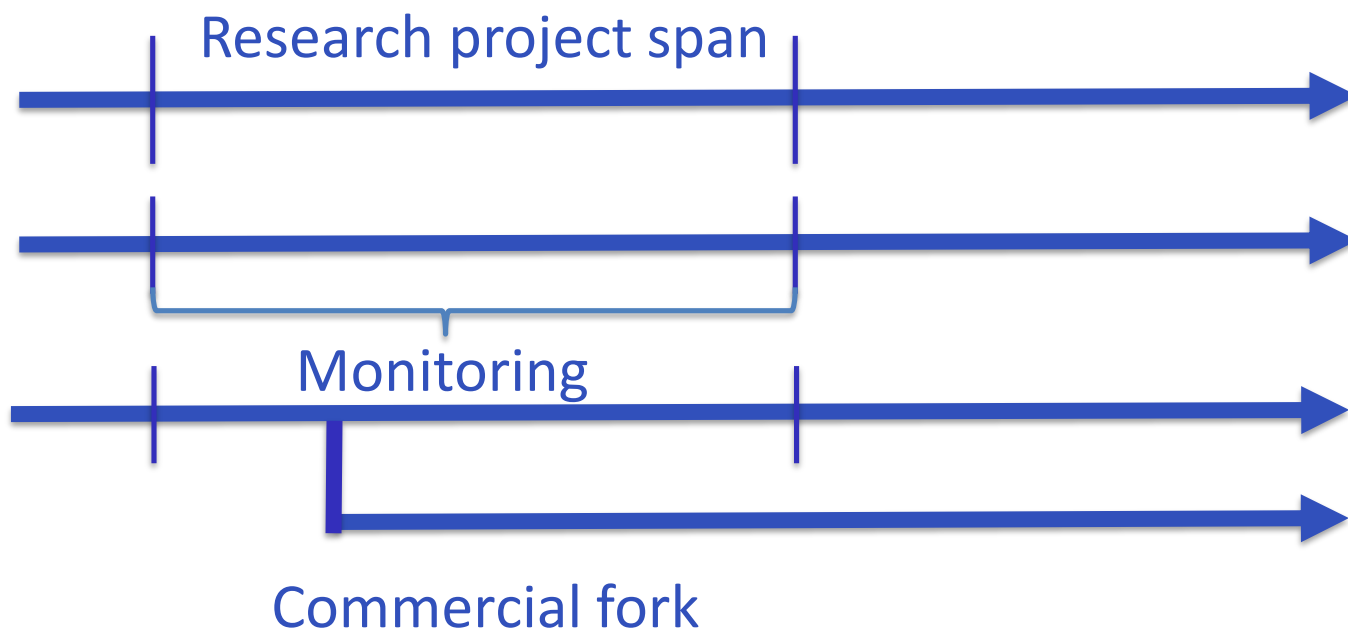
Best Practices in Online Training

- MOOCs: support multi-course programs, nano-degrees, micro-masters, specializations from different institutions
- MOOCs are typically used:--
 - Highlight *beacon areas of research*
 - To improve public understanding of science
 - Aid recruitment for traditional & distance learning courses
 - One MOOCs unit is equivalent to 1-1.5 ECTS credits



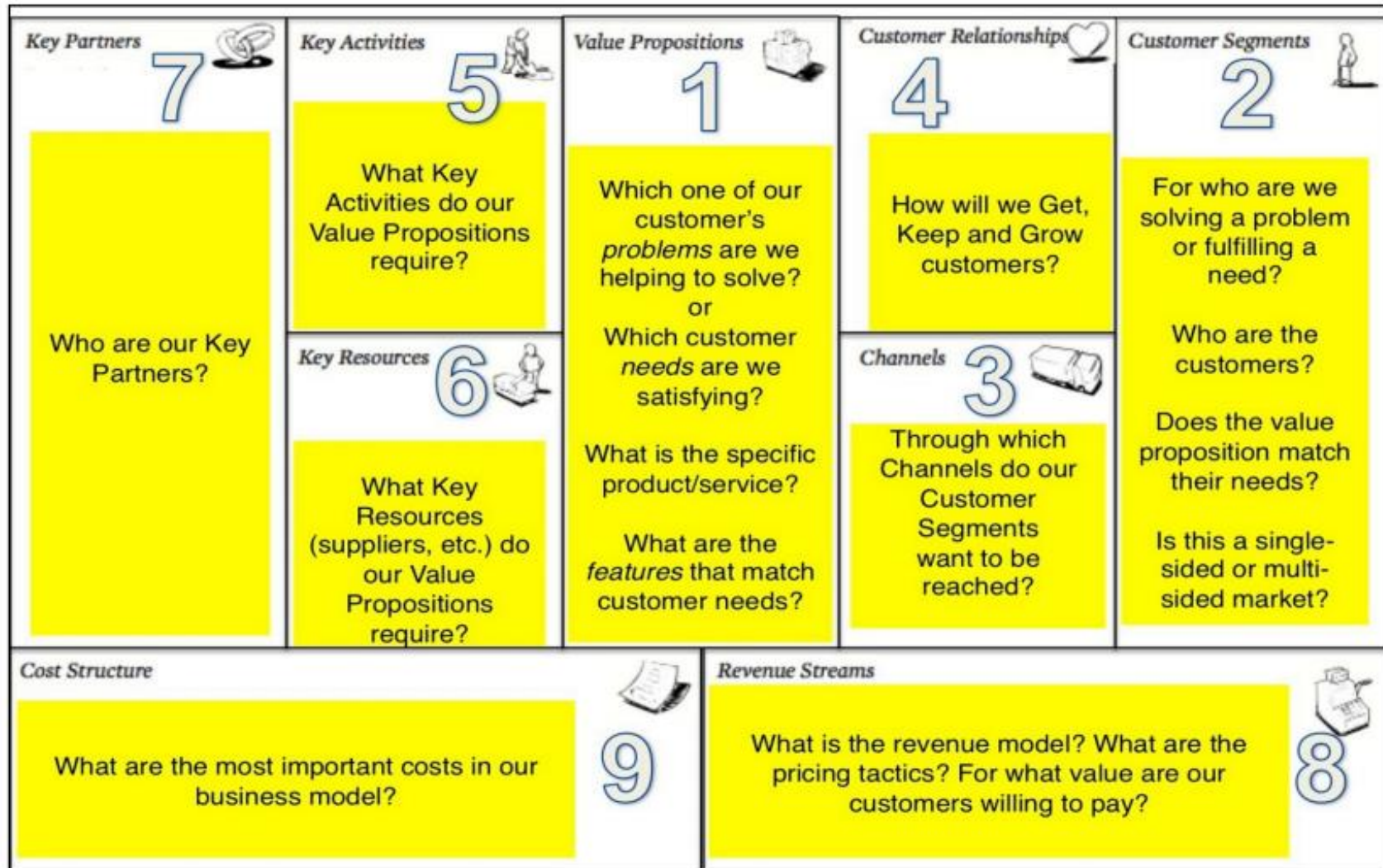
Acceleration of Innovation

Problem: Time to market of research ideas



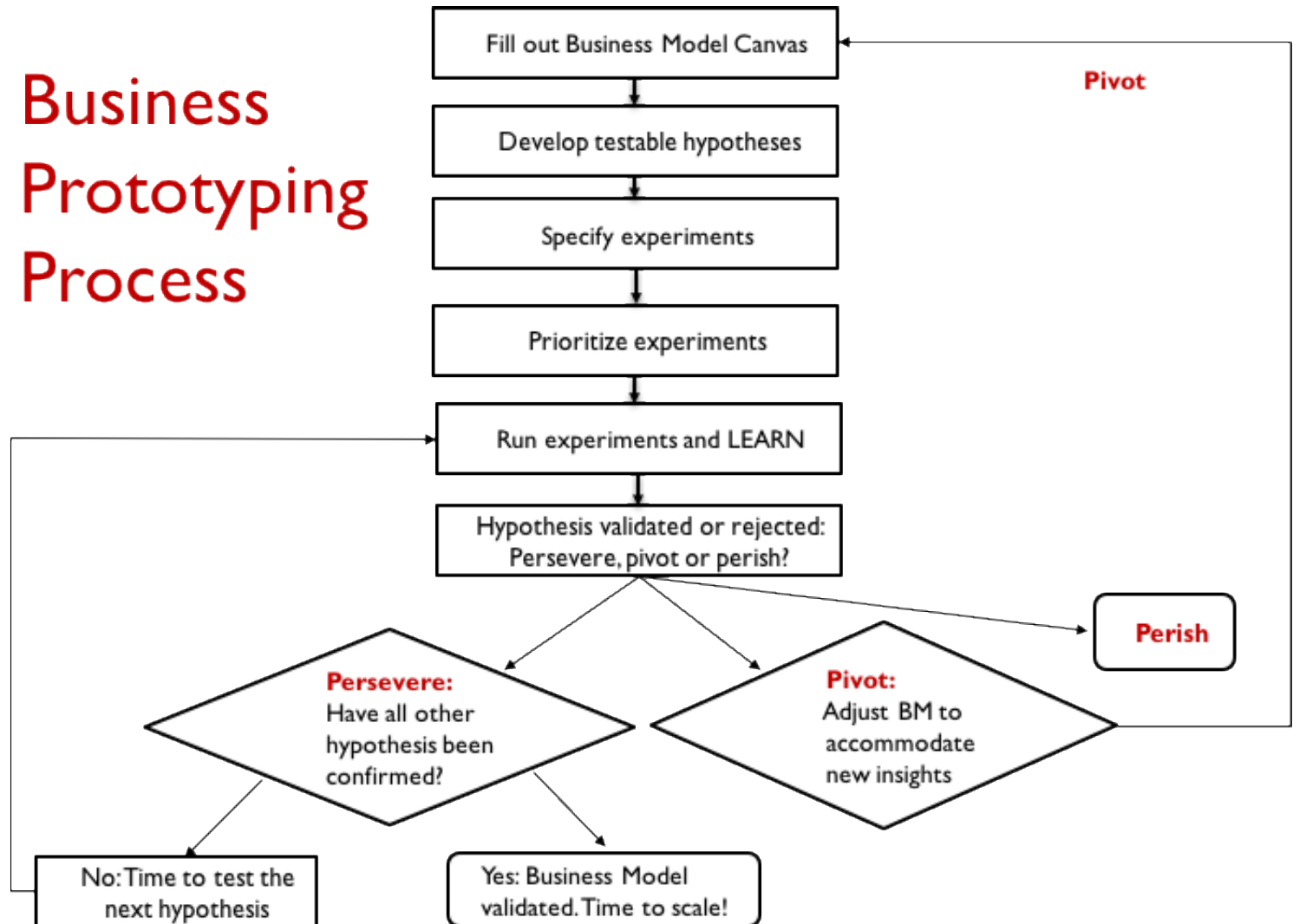
Outcome: Business prototyping – acceleration of uptake of research idea: Business prototyping

Business Model Canvas – Mapping Hypotheses



Business Prototyping – Testing Hypotheses

Business Prototyping Process





Community Building

- Common research platforms: vehicle for common research goals
- Instrument: Cross-site visit program
- Mechanism for linking communities to other communities

Outcome: Strengthening of links between research groups in HPC systems and between HPC stakeholder groups





Events Organized Year 1



EUROLAB-4-HPC

- EuroLab-4-HPC kickoff Milan Computer Systems Week, September
- HiPEAC 2016 Conference, January, Prague
- EuroLab4HPC Computer Systems Week Porto, April
- HPC Summit Prague, May





EUROLAB-4-HPC

HPC Summit Prague

- "Why is European HPC running on US Hardware? – EuroLab4HPC: Connecting HPC and Systems
 - Keynote: Creation of a European HPC Solution?, Prof. John Goodacre
 - 3 further talks

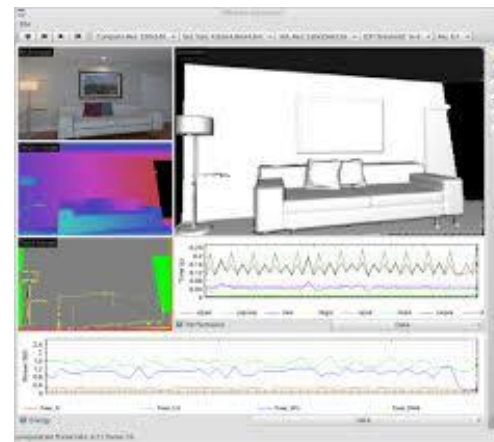




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Open-Source Activities

- Open source workshop in Porto
 - Holistic benchmarking in 3D Robot Vision: the SLAMBench open source framework, by Luigi Nardi, Imperial College London
 - Open Source Hardware: Our experience releasing the PULP platform, by Frank K. Gürkaynak, ETH Zürich





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New Applications

- CloudSuite 3.0:
 - Open-source, publicly available at Github
 - Add Big Data analytics (cloud convergence w/ HPC)
 - Integrated into Google PerfKit (supports all major cloud providers)
- Engagement: Four events
 - Keynotes, position talks, workshops, panel sessions
 - Tutorials at HiPEAC & EuroSys '16





Summary

EuroLab-4-HPC achievements

- **EuroLab HPC Vision:** a long-term research agenda
- A validated **HPC curriculum** and best practices
- Piloted **business prototyping** for accelerating innovations in HPC technologies
- **Ecosystem building:** Links to ETP4HPC, PRACE, EXDCI and other HPC stakeholder

EuroLab-4-HPC2 will strengthen all these efforts





Thank you!

www.eurolab4hpc.eu

